

ABSTRACT OF THE DISCLOSURE

Embodiments of the invention provide a memory command and address (CA) bus architecture that can accommodate higher CA data output frequencies with reduced signal degradation. For one embodiment of the invention the CA signal is routed to a first of two dual in-line memory modules (DIMMs) of a two-DIMM/channel memory bus design. The CA signal is then divided into components, with each CA signal component routed serially through a group of dynamic random access memory (DRAM) chips on the first DIMM. The CA signal components are then recombined and routed to the second DIMM. The recombined CA signal is then divided again into components, with each CA signal component routed serially through a group of dynamic random access memory (DRAM) chips on the first DIMM and the CA signal components are then recombined. In one embodiment, after routing through each DRAM, the CA signal is terminated on the DIMM.